In the Claims:

Please **amend** Claims 1, 7, 11, and 12 by substituting the following:

1. (Twice amended) An integrated circuit chip having an on-chip multi-layer metal-shielded monolithic transmission line comprising:

a plurality of parallel planar thin film conductive layers; and

a plurality of planar thin film nonconductive separator layers disposed such that each adjacent pair of the conductive layers is separated by at least one of said plurality of planar thin film nonconductive layers to provide a stack of alternating conductive and nonconductive layers,

wherein an initial one and a final one of said conductive layers provide a top conductive plane and a bottom conductive plane,

wherein a center one of the conductive layers comprises three laterally spaced apart conductive strips, said conductive strips separated by nonconductive material such that two laterally spaced terminal strips of the three conductive strips are spaced at a selected width from the center conductive strip,

wherein each of the nonconductive separator layers include a plurality of vias between the two laterally spaced terminal conductive strips of the three conductive strips and the top and bottom conductive planes, said plurality of vias filled with conductive material, and

wherein the distance between the top and bottom conductive planes is substantially equal to the distance between the two laterally spaced terminal conductive strips.

11. (Twice amended) An integrated circuit chip having a plurality of on-chip multi-layer metal-shielded monolithic transmission lines comprising:

a plurality of parallel planar thin film conductive layers, each adjacent pair of the conductive layers separated by at least one of a plurality of planar thin film nonconductive separator layers to provide a stack of alternating conductive and nonconductive said layers,

wherein an initial one and a final one of said conductive layers providing a top conductive plane and a bottom conductive plane,

BY wherein one of the conductive layers between the top and the bottom conductive planes includes a plurality of N laterally spaced apart conductive strips, where N is an odd integer,

wherein each laterally adjacent pair of the conductive strips are separated at a predetermined width by nonconductive material,

wherein the plurality of nonconductive separator layers include a plurality of metal filled vias positioned for electrically interconnecting every other one of the laterally spaced apart conductive strips to the top an bottom conductive planes, and

wherein the distance between top conductive plane and bottom conductive plane is substantially equal to the distance between every other laterally spaced conductive strips .